NOVATEUR PUBLICATIONS
International Journal Of Research Publications In Engineering And Technology [IJRPET]
ISSN: 2454-7875
VOLUME 2, ISSUE 10, Oct. -2016

A NOVEL MODIFIED CASCADED MULTILEVEL INVERTER WITH OPTIMAL NUMBER OF CONSTANT ACTIVE SWITCHES

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ABSTRACT:

As of late utilization of multilevel inverters (MLI) are expanded for high power mechanical applications. This paper introduces a changed cascaded MLI for 31-levels utilizing optimal number of constant active switches at any given purpose of time. The circuit comprises of arrangement associated sub cell which are utilized to deliver positive levels. H-extension is further associated with circuit to create alternative waveform. Power supply of this circuit is in binary arrangement. Voltage balancing issue is comprehended by utilizing this setup. Selective Harmonic Elimination is utilized to ascertain the switching pulses for MOSFETS. MATLAB/SIMULINK is utilized for logical investigation of the circuit.

KEYWORDS: Sub cell, asymmetric supply, binary configuration, optimal number of constant active switches, voltage balancing

INTRODUCTION

Presently a day's multilevel inverter assumes an essential part in numerous mechanical and high power applications. It has the preferences like low dv/dt and di/dt stress over the switch and low EMI is watched. It utilizes different low voltage sources to create high voltage yield. This component gives the application in renewable vitality sources like sun based and energy units. They got yield waveform from MLI is almost sinusoidal which has better power quality.

Cascaded H-Bridge inverter is fundamental multilevel inverter which has points of interest like measured quality, low push over the switches, quality yield waveforms. Be that as it may, it needs more number of switches; misfortunes are high, size, and cost of the circuit more. It has the voltage balancing issue because of more number of switches.

This paper presents adjusted cascaded MLI. It comprises of various sub cells by which it can deliver positive levels, further H-bridge is utilized to create the positive and negative half cycles. This has the benefit of optimal number of constant active switches at any given purpose of time. The circuit is supplied with unsymmetrical voltage sources which are in binary design. This can take care of the voltage balance issue present in Cascaded H-Bridge MLI.

LITERATURE REVIEW:

Multilevel inverters are considered today as a attractive solution for medium-voltage, high power applications. In fact several major manufacturers commercialize Neutral Point Clamped (NPC), Flying Capacitor (FC) or Cascaded H-Bridge (CHB) topologies with a wide variety of control methods [1]. Multilevel inverters have the advantage of low dv/dt and low di/dt during switching. The quality of output is improved and having low THD.

The voltage sources can be configured in different ratios, sources may be symmetrical or asymmetrical. In symmetrical all sources values will be same. In asymmetrical configuration sources may be in binary or trinary configuration. This gives the advantage of having more voltage levels with less number of sources. Another advantage of asymmetrical configuration is we obtain less THD values [2, 3]. In CHB configuration, due to more number of switches, charge unbalance problem may occur; this problem can be resolved by using duty cycle swapping method [4]

Different topologies have been proposed with reduced number of switches [5, 6]. In symmetrical configuration the topology needs more number of switches, with this the efficiency decreases, complexity and cost of the system increases. With asymmetrical configuration we can overcome these problems.

The control signals to switches can be given by using different modulation techniques [7] such as Fundamental Frequency Switching, Multicarrier Pulse Width Modulation, and Space Vector Modulation. Fundamental frequency switching has the advantage of less switching losses.

PROPOSED MODIFIED CASCADED MULTILEVEL INVERTER:

The modified cascaded MLI is as appeared in Fig 1. As appeared in figure it comprises various sub cells. All sub cells are associated as appeared in the Fig 1. Each sub cell is as appeared in Fig 2. Each sub cell comprises of two voltage sources. The voltage source can be a renewable vitality sources like nearby planetary group, energy units or any capacity gadgets like batteries, capacitors. Every cell comprises of four switches in that two switches L_{2n} and L_{3n} are unidirectional switches. L_{1n} and L_{4n} are bidirectional changes which need to with stand with both positive and negative voltages. With the utilization of inductive burdens reverse streams may happens with that the changes need to withstand. With the assistance of cascaded sub cells it can create positive levels. H-extension is associated with it to produce both positive and negative polarities, P_1 and P_2 will lead amid positive half cycle P_3 and P_4 will direct amid negative half cycle. More number of steps can be acquired. Because of this it can create about sinusoidal waveform which enhances the power quality. The configuration procedure is examined in further segments. The switching table is as given in Table 1. For positive yield levels in that P_1 and P_2 are on for negative yield levels P_3 and P_4 will direct. From the switching table we can watch that the quantity of directing switches are same at any moment of time.

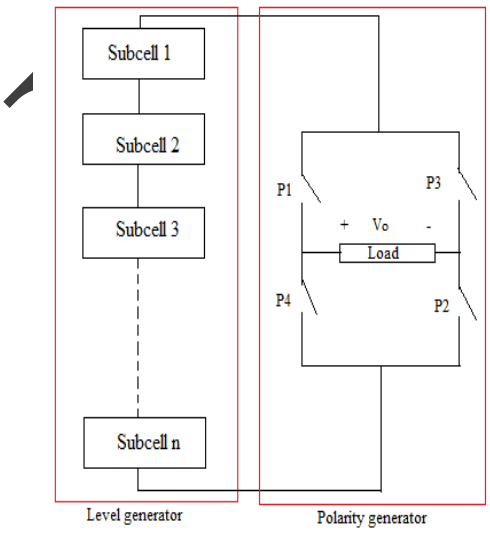

Fig. 1. Modified cascaded multilevel inverter

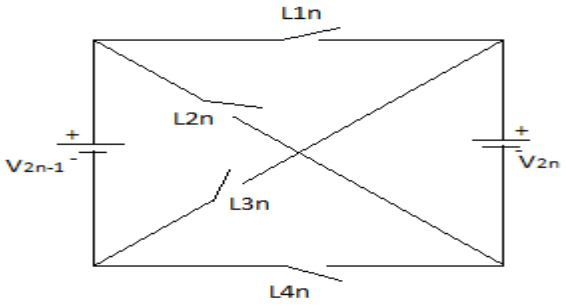

Fig. 2. Subcell

Table 1 Switching states of binary configuration

L1	L2	L3	L4	L1	L2	L3	L4	Lev
0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	1	0	1
0	0	0	1	0	0	1	0	2
0	1	0	0	0	0	1	0	3
0	0	1	0	1	0	0	0	4
1	0	0	0	1	0	0	0	5
0	0	0	1	1	0	0	0	6
0	1	0	0	1	0	0	0	7
0	0	1	0	0	0	0	1	8
1	0	0	0	0	0	0	1	9
0	0	0	1	0	0	0	1	10
0	1	0	0	0	0	0	1	11
0	0	1	0	0	1	0	0	12
1	0	0	0	0	1	0	0	13
0	0	0	1	0	1	0	0	14
0	1	0	0	0	1	0	0	15

DESIGN OF MODIFIED CASCADED MLI:

The proposed circuit requires 2k+4 switches for the given k DC voltage sources. The following (1) gives the relation between number of DC voltage sources and sub cells

$$n=k/2 \quad (1)$$

$$N_{sw}=2k+4 \quad (2)$$

In symmetrical configuration all voltage sources are equal

$$V_1=V_2=V_3=\ldots\ldots\ldots\ldots=V_n \quad (3)$$

In the proposed topology the voltage sources V_1, V_2, V_3 ……. V_n relation in general given by the (4)

$$V_i = r^{m-1}V_{DC} \quad (4)$$

Where i=1,2,3……k, r is the ratio factor of the voltage sources in binary configuration r=2

The total output voltage of the given topology is given by the (5)

$$V_{out}= \pm(V_{01} + V_{02} + \cdots \ldots \ldots \ldots \ldots \ldots + V_{0n}) \quad (5)$$

The maximum output voltage for a given voltage ratio factor given by the (6)

$$V_{out\ max} = \left(\frac{r^k-1}{r-1}\right) V_{DC} \quad (6)$$

The number of voltage levels that can be generated in general given by the (7)

$$N_{out\ level} = 2 * \left(\frac{r^k-1}{r-1}\right) + 1 \quad (7)$$

The reverse blocking voltage of nth basic sub cell given by the (8)

$$V_{b\ nth\ subcell} = V_{b\ L1n} + V_{b\ L2n} + V_{b\ L3n} + V_{b\ L4n}$$
$$V_{b\ nth\ cell} = 2V_{2n-1} + 4V_{2n} \quad (8)$$

The reverse blocking voltage of total circuit given by the (9)

$$V_{b\ circuit} = \sum_{i=1}^{n} (2V_{2i-1} + 4V_{2i}) \quad (9)$$

A. *Snubber Circuit Design*

Turnoff snubber arrangement is used to obtain zero voltage across the switch when current goes to zero [8]. The value of snubber circuit elements are given by the (10) and (11)

$$R_s = 5 * \frac{V_d}{I_O} \quad (10)$$

$$C_s = \left(\frac{I_o * t_f}{2 * V_d}\right) \quad (11)$$

Where R_s is turnoff snubber resistor, C_s is turnoff snubber capacitor. C_s is used to limit dv/dt during switching.

B. *Total harmonic distortion:*

The important performance factor for a inverter is total harmonic distortion (THD) [9]. For the sinusoidal waveform, the THD is defined as follows

$$THD = \sqrt{\left(\frac{V_{o\ rms}}{V_{01}}\right)^2 - 1} \quad (12)$$

Where $V_{o\ rms}$ represents the rms magnitude of the output voltage. In the above relation, the values of V_{01} and V_{orms} can be obtained using the following equations respectively.

$$V_{orms} = \frac{2\sqrt{2}V}{\pi} * \sqrt{\sum_{m=1,3,5,\ldots..}^{\infty} \left(\sum_{j=1}^{N_{level}} \frac{\cos(m\theta_j)}{m}\right)^2} \quad (13)$$

$$V_{01} = \frac{2\sqrt{2}V}{\pi} * \sqrt{\sum_{j=1}^{N_{level}} \cos(\theta_j)} \quad (14)$$

Where the values of $\theta_1, \theta_2, \theta_3, \ldots\ldots\ldots\ldots, \theta_{N\ level}$ represents switching angles are obtained by (15) for the given values j=1, 2, 3, ……, N_{level}

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{level}}\right) \quad (15)$$

SIMULATION RESULTS:

The proposed topology is simulated using MATLAB/SIMULINK. The DC voltages used are V_1=24v, V_2=48v, V_3=96v, V_4=192v. Various output voltage levels are generated as per switching table1. Switches P_1, P_2 are used to produce positive half cycle, switches P_3, P_4 are on for complimentary half cycle i.e for negative half cycle. Simulation was done for RL load with values 40ohm, 40mH. Frequency of output voltage is 50HZ. Switching pulses are given to MOSFETS by Selective Harmonic Elimination method. Simulation diagram is as shown in the Fig. 3.

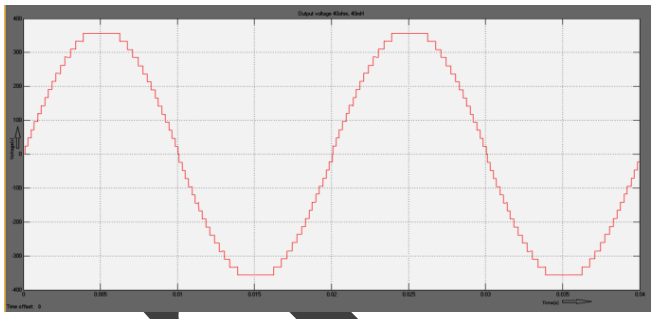

Fig. 3. Simulation diagram

Fig. 4. and Fig. 5. shows the 31 level modified cascaded MLI simulated output voltage waveform and output current waveform respectively for RL load with the values 40ohm, 40mH. Current waveform is close to sinusoidal waveform even without using the passive filters. It is also clear that there is phase difference between voltage and current waveforms.

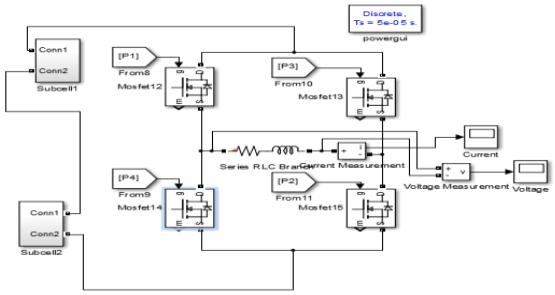

Fig. 4. Simulated output voltage waveform of 31-level inverter

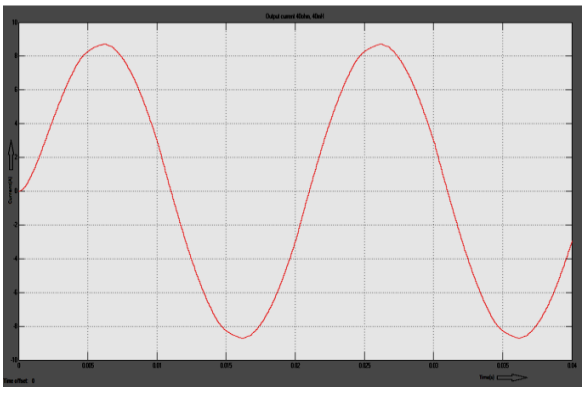

Fig. 5. Simulated output current waveform of 31-level inverter

Fig. 6. shows the FFT analysis of the 31 level MLI output voltage waveform. The THD value is 3.51%. Fig. 7.

shows the FFT analysis of the 31 level MLI output current waveform. The obtained THD value is 2.72%. Obtained THD values are less than IEEE standards (i.e < 5%) without using passive filter.

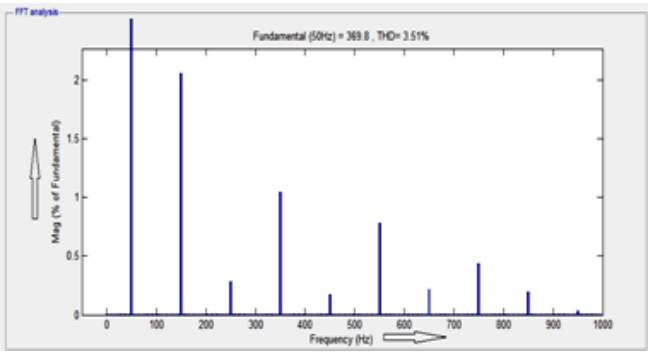

Fig. 6. FFT analysis of simulated output voltage waveform

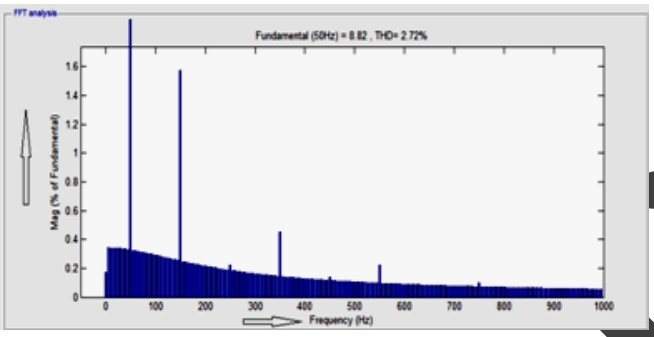

Fig. 7. FFT analysis of simulated output current waveform

CONCLUSION:

The proposed modified cascaded MLI utilizes constant active number of switches. Yield waveform quality is acquired with the high number of levels. They got THD of voltage waveform is 3.51%, THD of current waveform is 2.72% which are less than IEEE standard (i.e < 5%) without utilizing detached channel. The upside of this topology is

- Circuit is basic and secluded.
- Used ideal steady number of dynamic switches.
- Voltage unbalancing issue dispensed with.

The productivity of the circuit is enhanced with the utilization ideal number of switches and gate drivers, which in-turn lessens the size, cost and control many-sided quality of the circuit.

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