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PERFORMANCE ENHANCEMENT OF 8 BIT RISC ARCHITECTURE

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Abstract— In this paper we have selected PIC16A84 processor as base platform for the enhancement of its features. Selected processor is based on the 8bit RISC platform. The intention is to enhance the capabilities of the soft-core in terms of 16 bit arithmetic operations. Addition of new blocks tested by adding the new instruction in the instruction set.

Keywords— CALU; RISC;

I. INTRODUCTION

A *microprocessor* is one of the most central parts of a modern personal computer or, in fact, any advanced computer device. The invention of microprocessor was done by late 1960s. The journey were started with 4 bit processors like Intel 4004, TMS 1000. Later Intel developed the popular 8 bit architectures like 8085, 8086, 80268, X86 and so on. The development of microprocessors has brought us so far, so that microprocessors have became part of every device of our day to day life. Today's microprocessors are so much powerful as well as power efficient too. Due to capability of handling very large amount of data, the application of microprocessor have reached every area on the planet.

We are at beginning of the new era of "Internet of Things", where each and every thing will be connected to the internet. Applications in the field of IOT demand the processors for handling the node data and communication with the network. Also it demands very low power chips that can be operated on battery or battery less.

The development of the microprocessor is continuously evolving journey.The architecture has been modified as per increasing demand of the high density chips, high speed computations, and low power applications. While fulfilling the requirements, there has been made some tradeoff compromises. So keeping the objective of reducing these tradeoffs, this dissertation has been proposed. The development of Soft computation engine will be able to enhance the performance of the 8 bit computation engine in terms of the speed, throughput, removing pipeline issues, reduction in rollback time etc. These enhancements will be done on the very popular PIC architecture. The proposed architecture will have two new blocks in the architecture. The block CALU (Co-operative ALU) will be responsible for the enhancement of the ALU operations.. The addition of the block, desired to enhance the performance of the existing architecture.

II. LITERATURE REVIEW

Following is a list few recent researches carried out in the field of microprocessor design.

Xin Liu, Kah-Hyong Chang, [1] have presented an energy-efficient sensor node processor (SNP) is presented for intelligent sensing in Internet of Things (IoT) applications. To achieve ultralow energy consumption and satisfying performance, the proposed processor incorporates an ARM Cortex-M0 RISC core and diverse hardware accelerators, including discrete wavelet packet transform engine, finite-impulse response filtering engine, fast Fourier transform engine, and coordinate rotation digital computer engine, to accelerate signal processing tasks. At the architecture level, dual-bus architecture with automatic bus sensing and reconfigurable memory access scheme are proposed. At the circuit level, digitally assisted cognitive sampling and ultralow-voltage operation with in situ timing error monitoring techniques are employed. When applied to neural spike classification and vehicle speed detection, the proposed SNP consumes only 39 and 29 pJ/cycle, respectively.

Oluleye D. Olorode, [2] have presented on Cache memory systems. Cache memory systems consume a significant portion of static and dynamic power consumption in processors. Similarly, the access latency through the cache memory system significantly impacts

the overall processor performance. Several techniques have been proposed to tackle the individual power or performance. However, almost all trade off performance for power or vice versa. He has proposed a novel scheme that improves performance while reducing both static and dynamic power with minimal area overhead. The proposed scheme reduces dynamic power by using a hash-based mechanism to minimize the number of cache lines read during program execution. This is achieved by identifying and not reading those that are guaranteed non-matches (i.e., cache misses) to a new access. Performance improvement occurs when all cache lines of a referenced set are determined non-matches to the requested address, and therefore skip a few cache pipe stages as guaranteed misses. Static power savings is achieved by exploiting in-flight cache access information to deterministically lower the power state of cache lines that are guaranteed not to be accessed in the immediate future. These techniques easily integrate into existing cache architectures and were evaluated using widely known CAD tools and benchmarks. We have observed up to 92, 17, and 2 percent improvements in performance, static, and dynamic power, respectively, with less than 3 percent area overhead.

Yuki Ando, Ryo Sato, Masamitsu Tanaka [3], have design their own 8-bit bit-serial rapid single-flux-quantum (RSFQ) microprocessor, which is called CORE e4. The CORE e4 is equipped with four general-purpose registers and can execute 20 different instructions. The CORE e4v1 occupies a circuit area of of 3.00 mm X 1.98 mm. The estimates power consumtion is 2.03mW and performance is 333 million instructions per second. Core e4 is one of the high performance RSFQ microprocessors

Kaisheng Ma, Xueqing Li [4], have presented for non volatile processor architecture for exploration energy-harvesting systems. They provided the architectural solution for very low power operation of the microprocessor, such that we use the Solar panels, RF Receivers, Vibration Sensors or thermoelectric devices as power source of the system. The optimization of the processor latency and throughput has been done by providing various ways to reduce the time in Storage and retrieval time of the processor registers when the power fluctuations or power cut occurs. The lesser time in storage and retrieval ultimately leads to low power consumption as well as high speed operation. They provided the Backup solutions: when to backup, what to backup, How to backup, Where to backup.

Avinash Patil, Y. V. Chavan, Sushma Wadar [5] has presented the survey of performance of the Vedic multiplication techniques. They have implemented the multiplier using ancient vedic techniques such as Nikhilam sutra, ekadhiken purven sutra and Urdhva – Tiryagbhyam sutra. The implementation has found better than conventional on the ground of number of digits, number of gates and time requires.

After doing the above literature survey it is decided that to develop 8 bit RISC Soft Computational Engine using few of the above concepts such as Vedic techniques for ALU design, Non-volatile architecture for low power consumption.

III. PROPOSED WORK

The generalize architecture of the proposed Soft Computational Engine is as shown in above block diagram. It consists of traditional blocks like ALU, Program Memory, Register Array, Timing & Control Unit, Pipelining etc.

In the proposed system we have coined two new terms called CALU and FAS. CALU stands for the Co-operative ALU, which is responsible for acceleration of ALU processes in special cases. Then another term we are introducing is FAS, FAS stands for Flushing Avoidance System. The FAS unit is responsible to avoid the various hazard occurring in the pipelined architecture.

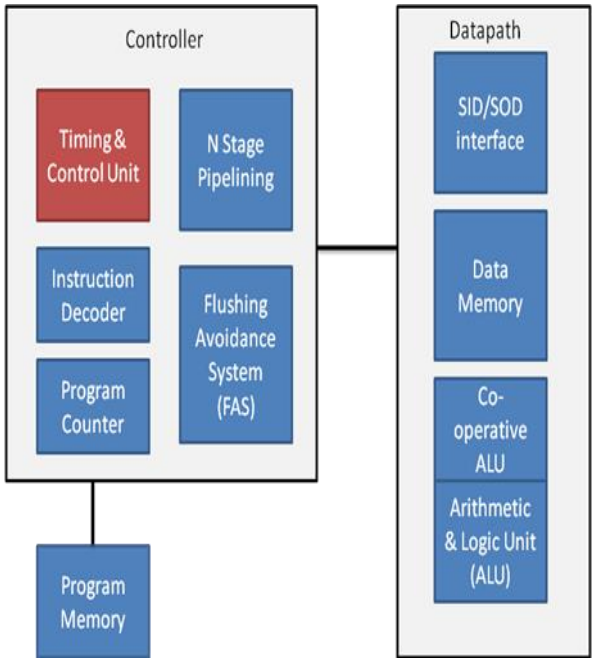

Fig.1 :Soft Computational Engine Architecture

A. Cooperative ALU

The Cooperative ALU is new term introduced here in order to enhance the capabilities of the 8 bit microprocessor. This block will be responsible for performing 16 bit arithmetic operations.

CALU consist of the 16 bit carry select adder as its core element.

Selection of Carry Select Adder is done by comparison with other adders on basis of time required, chip area, power consumption. CSelA was selected for its lowest computation time.

Along with the CSelA the dedicated register for storing input operands and results are introduced in Data memory organization.

Implementation and Simulation of CSelA:

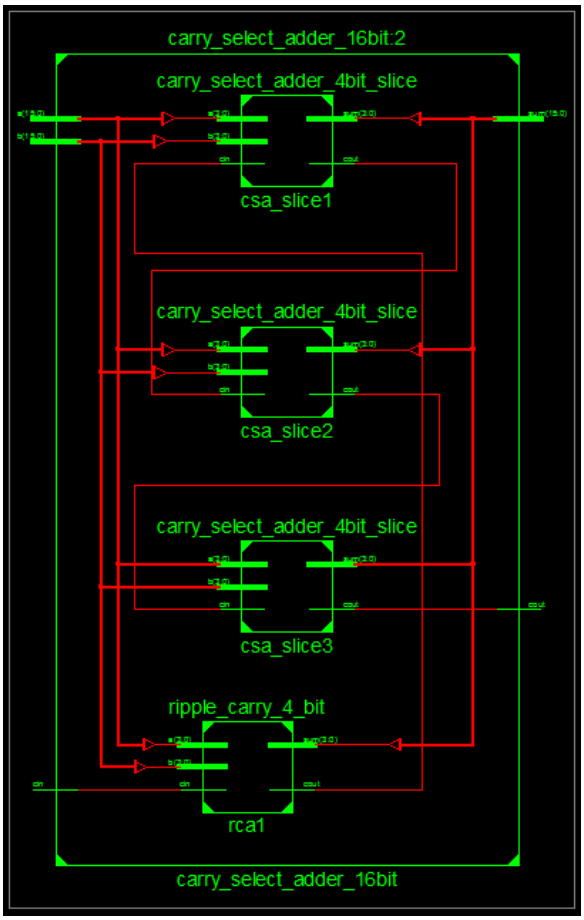

Fig. 2: Implementation of CSelA

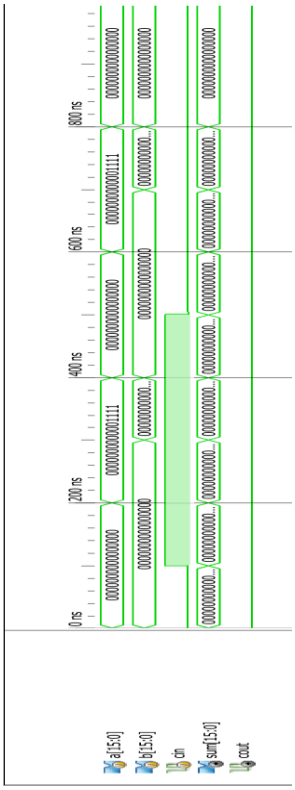

Fig. 3: Simulation Results of CSelA

II. RESULT AND DISSCUSSION

Execution of instruction for addition & substraction of word i.e 16 bit is simulated in Xilinx 14.1. The functional testing results are given as follws:

Instruction: ADD16

Description: Performs the 16 bit addition on the dedicated registers as an input and stores result in dedicated output registed called CALU Out.

Opcode: 100011100001100

Flags Affected: Carry, Zero, Auxilary Carry

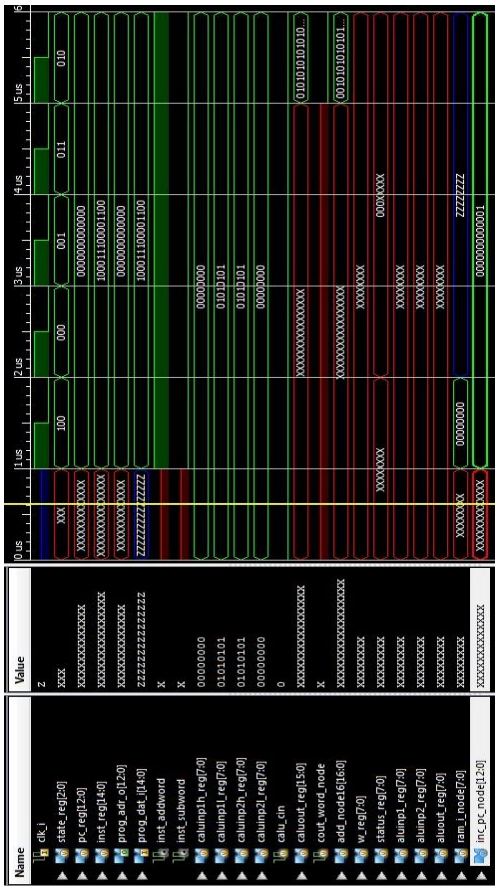

Fig.4 :Simulation of ADD16 instruction

Instruction: SUB16

Description: Performs the 16 bit substraction on the dedicated registers as an input and stores result in dedicated output registed called CALU Out.

Opcode: 100011100001100

Flags Affected: Carry, Zero, Auxilary Carry

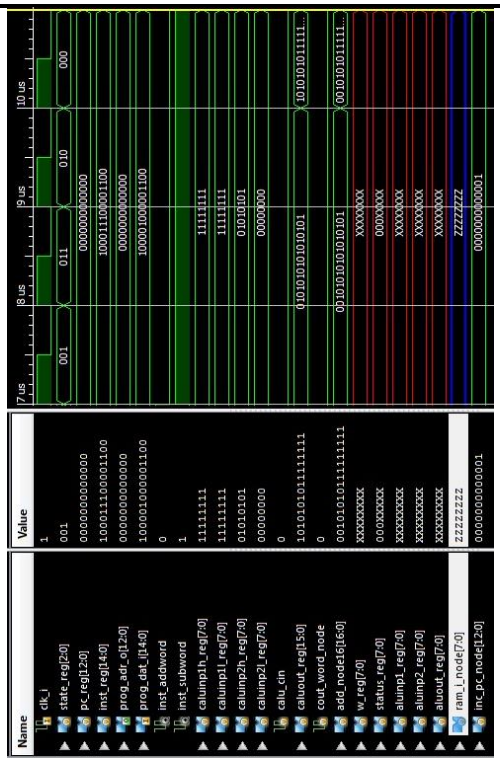

Fig.5 :Simulation of SUB16 instruction

Performance improvement:

16 bit addition/subtraction on original core:

assuming all operands are kept in data memory requires 6 clock cycles.

MOVF 30h,0;

ADDWF 32h,1;

MOVF 33h,0;

BTFSC 03H,0;

ADDLW 01h;

ADDWF 31h,1;

16 bit addition/subtraction on enhanced core:

assuming all operands are kept in data memory requires only 1 clock cycle.

ADD16;

here 5 clock cycles are saved. This will lead to reduction of power consumption.

Total Power Consumption for Enhanced Core: 83.94 mW

Max Clock frequency: 29.95 MHz

V. CONCLUSION

Execution of instruction added for the cooperative arithmetic and logical unit is simulated for function testing successfully in Xilinx 14.1 and Isim. The execution of instruction is completed within the single clock cycle as per RISC architecture constraint. The performance improvement has been recorded in terms of the clock cycles savings.

VI. REFERENCES

[1] Xin Liu, Jun Zhou, Chao Wang, Kah-Hyong Chang, Jianwen Luo, Jingjing Lan, Lei Liao, Yat-Hei Lam, Yongkui Yang, Bo Wang, Xin Zhang, Wang Ling Goh, Tony Tae-Hyoung Kim and Minkyu Je , "An Ultralow-Voltage Sensor Node Processor With Diverse Hardware Acceleration and Cognitive Sampling for Intelligent Sensing", presented in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 62, NO. 12, DECEMBER 2015

[2] Oluleye D. Olorode and Mehrdad Nourani, "Improving Cache Power and Performance Using Deterministic Naps and Early Miss Detection" presented in IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, VOL. 1, NO. 3, JULY-SEPTEMBER 2015

[3] Yuki Ando, Ryo Sato, Masamitsu Tanaka, Kazuyoshi Takagi, Naofumi Takagi, and Akira Fujimaki, "Design and Demonstration of an 8-bit Bit-Serial RSFQ Microprocessor: CORE e4", presented in IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, VOL. 26, NO. 5, AUGUST 2016

[4] Kaisheng Ma, Yongpan Liu, Jack Sampson, Vijaykrishnan Narayanan, "Nonvolatile Processor Architecture Exploration for Energy Harvesting Applications", presented Article in IEEE Micro · September 2015

[5] Avinash Patil, Y. V. Chavan, Sushma Wadar, "Performance analysis of multiplication operation based on vedic mathematics" presented in 2016 International Conference on Control, Computing, Communication and Materials (ICCCCM), IEEE 2016

[6] R.UMA,Vidya Vijayan, M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies" presented in International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012

[7] M. Prakash , C.Bhargav, K.PrasadBabu , H.Devanna, K.Sudhakar, "Design of Low Power 8-bit Carry Select Adder" presented in International Journal of Scientific Engineering and Applied Science (IJSEAS) - Volume-1, Issue-6, September 2015