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RECONFIGURABLE HARDWARE IMPLEMENTATION OF FUSED ADD-MULTIPLY OPERATOR

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ABSTRACT:

Arithmetic operations are now a days used in digital signal processing applications.Here we will focused on implementation of fused add multiply operator. For getting recoding of sum of two numbers we will implement a technique called sum of two numbers in its modified booth. We introduce three different types of recoding technique. For using actual recoding technique we will compare with Fused add multiply designs. Here the technique which will be used that reduced some factors like delay, complexity ofhardware and power consume of the Fused add multiply unit.

KEYWORDS: A-M operation, Differentarithmetic circuit, Modified Booth recoding techniques.

INTRODUCTION:

In modern consumer electronics devices, Digital signal processing system is used which is providing Different technique for the Different multimedia and communications applications. A complicated digital signal processing technology have perform the different arithmetic operations and there implementation is based on different computational kernels, which are many techniques Fast Fourier transform, Discrete cosine transform, Finite impulse response filter and signals convolution. Performance of digital signal processing system are effected when they are doing the many complicated operations and the design which are considered for arithmetic operations. The research which are carry out now a days in which the operations which are carried out by the digital signal processing technique are so complicated. That is sharing of data and different operations In all the techniques the addition and multiplications are most hard operations Which may be done by Finite impulse response filters. The Multiply and multiply accumulator these two techniques are consider as a good techniques for implementing a digital signal processing systemsif we compare these with existing ones. Because they used very less sources. There are many techniques have been explain for implementing the multiply accumulator for reducing delay and critical path.

CONVENTIONAL MODEL:

As we seen there are many techniques and a technology has been introduced for implementing the most simple and sofestificated multiply Accumulators. Multiply accumulator increase the data path synthesis of digital signal processing systems. For doing large amount of arithmetic calculatiotions.There are many digital signal processing system which are based only on the Add multiply instead of multiplyaccumulator and the multiply add techniques.

Add multiply technique is so simple in this technique we simply providing the adders output to the multipliers input which is considers as an so simple technique and it is not applicable for many complicated arithmetic operatins.so it is better to avoid such simple techniques, will increases significantly area of the circuit and critical path delay of the circuit. It is actually increase the delay and critical path of the system, so it is an unacceptable technique for many complicated arithmetic operations. Now a day we require such a technique which takes less time and gives more output within respected time.

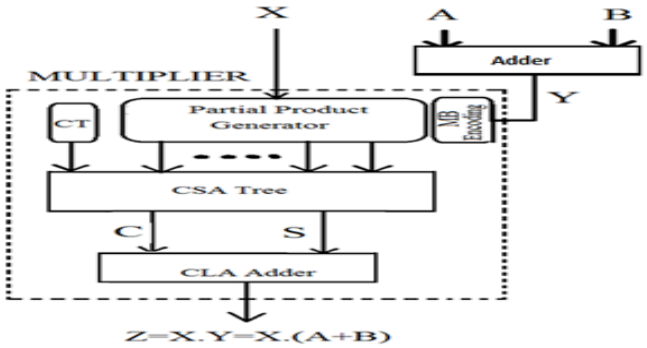

Fig 1.Existing Model

PROPOSED MODEL:

In proposed technique we are increasing the flexibility of Add multiply operator which is as just simple technique, inthis new model we are introducing the Fused technique actually which is depends on the sum of two numbers which comes in its modified booth. For sum of two numbers in its MB form needs to be implement a Fused add multiply operator as we compare it to its conventional form. This Fused add multiply technique

done some of best work which are it reduced the delay means time taken by the operation will be as reduced as possible and power will consume less and again the complex hardware design will also be simple. In fused add multiplytechnique with sum-modified booth recoding technique it is one of best technique Because it reduced the number of partial product and it also increase the calculation speed. It also decreases delay and reduces area and power which will be consumed. The technique which is sum to modified booth is an so simple technique which can be used for second compliment which we can say compliment of two and for unsigned numbers also. This can be comprised to odd and even bits. The new design of Add multiply operator is depend on fusion of adder and multiply encoding unit into a one data path. Block (Fig. 1) represent the direct recoding of the sum Y=A+B to its Modified booth design.

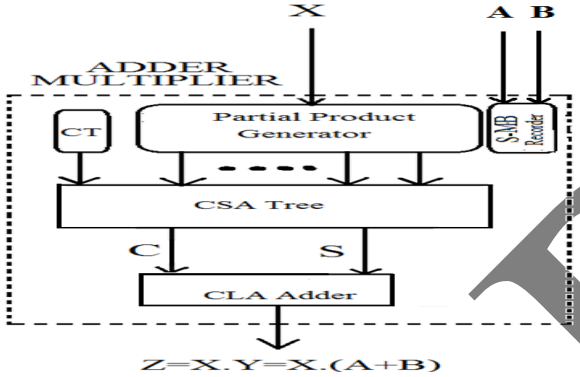

Fig 2. Proposed Model

The Above Diagramis fusedtechnique which representsthe direct recoding of the sum of and in its Modified Booth (MB) design. Here the multiplier which is used is an parallel multiplier to its modified booth form terms CT, carry save adder, and Carry look ahead adder these are used for the correction terms, the Carry-Save adder and last Carry look ahead Adder of the multipliers.

S-MB RECODINGTECHNIQUE:

Conventional Signed HA's and FA's are used to design alternative schemes of the three S-MB recodingtechniques. Each of the techniques can be applied in either signed and unsigned numbers which consist of odd or even number of bits. Consider that both the input A and B are in 2'nd complement form and it will consist of 2k bits in even case and 2k+1 in odd case to transform A and B(Y=A+B) in its modified booth representation those 3 SM-B scheme are,S-MB1,S-MB2 and S-MB3.

PERFORMANCE EVALUATION:

A.THEOROTICAL ANALYSIS:

In this section, we are analyzing and comparing the theoretical terms or factors. Here we are doing the observations based on three different techniques. Our observations will be on the basis of gate models. For our easy observation we will design on the basis on gates which are having only two inputs the gates are NAND, AND, NOR, OR.Here one gate will be equivalent of both area and critical delay. Area which will be taken by ha and fa equivalent to 3 and 7 gates. Sumof delay and carry which will be out is fa 4 and 3 gate. The whole design will be considered only on the full adder and the half adder.

B.EXPERIMENTAL EVALUATIONS:

Experimental Evaluations are depends on, comparisons of all the three techniques which will be used in the proposed technique. The programming which will be done for these techniques is an Verilog programming in vlsi.Experimental observations are on the basis of sum to modified techniques. Comparison will be carried out here for getting all results.

POWER MEASUREMENTS:

Below Tables are showing the different Measurements of power at all three recoding schemes that are S-MB1, S-MB2, S-MB3.

1)S-MB1

Table1.Power Measurement at S-MB1

Name	Power(inW)	Use	Available	Utilize
logic	0	2	1920	0.1
Signal	0	5		
IOS	0	5	6	7.6
Whole Quiescent Power	0.034			
Whole Dynamic power	0			
Whole power	0.034			

The table is of Power measurement at sum of modified booth recording technique (S-MB1). At logic the power will be 0 as same as on signal and IOS.The used power at logic is 2 and 5at signal ,again 5 at IOS.

Total Quiescent power is 0.034.Total available power at logic is 1920 at IOS it is 6 .The Utilization at logic is 0.1 and at IOS it is 7.6.

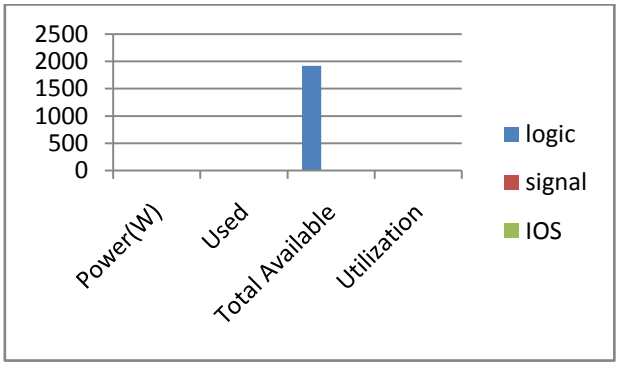

Fig 3.Power Measurement of S-MB1

2) S-MB2

Table2.Power Measurement of S-MB2

Name	Power(in W)	Used	Available	Utilize
clock	0	5		
logic	0	204	1536	33.3
signal	0	222		
IOS	0	45	124	36.3
Whole Quiescent Power	0.024			
Whole Dynamic power	0			
Whole power	0.024			

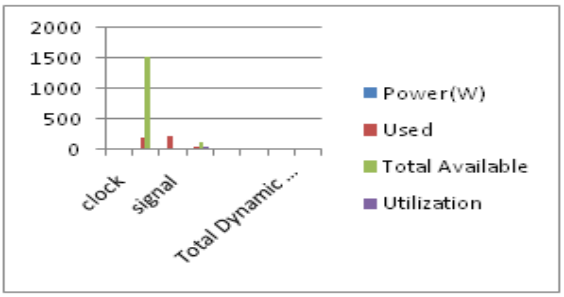

Fig 4.Graph for S-MB2

3) S-MB3

	Power(inW)	Use	Available	Utilize
Clock	0	4		
logic	0	412	1536	13.8
Signal	0	229		
IOS	0	44	124	35.5
Total Quiescent Pow.	0.024			
Total Dynamic pow.	0			
Total pow.	0.024			

Fig 7.Power Measurement at S-MB3

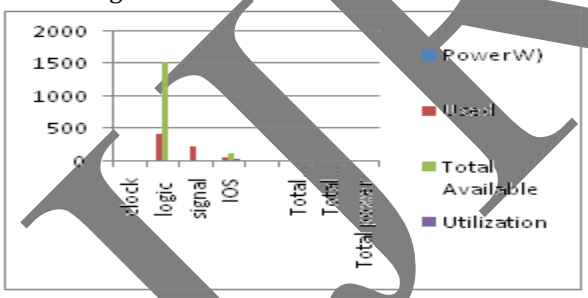

Fig 5.Graph at S-MB3

DELAY:

Table3.Delay Measurement

	Delay(ns)
SMB-1	17.91
SMB-2	16.463
SMB-3	17.025

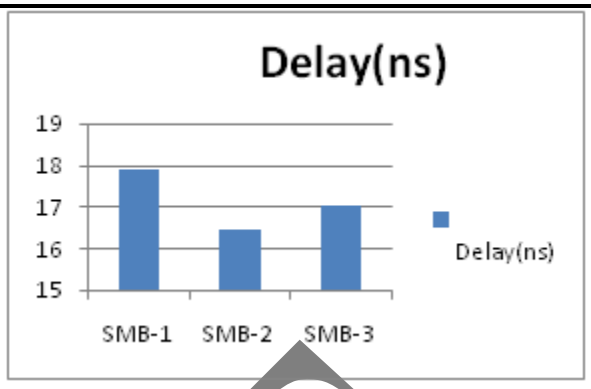

Fig 6.Graph for Delay Measurement

CONCLUSION:

Here we are comparing all the three techniques which are designed by using the newly suggested model. In this we are implementing the fused add multiply operator and than comparing all the techniques with the old technique which was depend on the only add multiply operator which was simple technique and taking more time for operations which are carried out by the existing technique. The technique which is used by us provides better results than previous which reduced the delay means taking less time, hardware design will simple.

REFERENCES:

1) Kostas Tsoumanis, Student Member, IEEE, Sotiris Xydis, Constantinos Efstathiou, Nikos Moschopoulos, and Kiamal Pekmestzi.VOL.61, NO.4, APRIL 2014.
2) Dr.B.Gopi1G.Kohila *Optimization of power in Fused Add Multiply Operator Using Modified Booth encoder*, Volume: 02 Issue: 02 May-2015.
3) V. Karuppasamy, S.Muthukumar '*Design of Low Power Digital Low Pass Filter Using FAM*' An ISO 3297: 2007 Certified Organization Vol.3, Special Issue 3, April 2015
4) M.Chitra Evangelin Christina P.MariaJothi Jenifer *An Efficient Design of Sum-Modified Booth Recorder for Fused Add-Multiply Operator* (IJIET) Volume 5 Issue 1 February 2015.
5) A.Sindhu, K.PriyaMeenakshi2 '*Implementation of Efficient Modified Booth recorder for Fused Sum-Product Operator*' Vol. 2, Issue 11, November 2014.
6) Y.-H. Seo and D.-W. Kim, *"A new VLSI architecture of parallelmultiplier–accumulator based on Radix-2 modified Booth algorithm,"*IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 18, no. 2, pp.201–208, Feb. 2010.