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DESIGN AND IMPLEMENTATION OF 8-BIT VEDIC MULTIPLIER

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ABSTRACT
Today's technology has raised demand for fast and real time signal processing operation. Multiplication is one of the most important arithmetic operations. In this paper, we have proposed design of vedic multiplier using "Urdhva Tiryagbhyam" sutra in Xilinx ISE. This design takes lesser time for operation than currently available multipliers .It encompasses wide era of image processing and digital signal processing in much efficient way with increase in speed and thus leading to higher performance rating
KEYWORDS: Vedic Multiplier, Urdhva Tiryagbhyam, Digital Signal Processing, Image processing

I. INTRODUCTION

Multiplication is very basic and primary operation used in digital signal processing, image processing and microprocessor. With increased and rapid progress in technology, we require operations to be done at faster rate. This need is fulfilled by use of Vedic multiplier which is derived from storage house of knowledge "Vedas".Swami Bharti Krishna Maharaja(1884-1960) is the one who derived vedic mathematics after deep study of eight years. Vedas are mainly based on sixteen sutras and thirteen subsutras. It also includes theory of numbers, compound multiplication, algebraic operation, calculus, squaring, cubing, cube root, simple quadratic, coordinate geometry and wonderful Vedic Numeric Code.The use of vedic multiplier improves speed of operations gives better efficiency in area of digital signal processing ,image processing and microprocessor.

URDHVA-TIRYAKBHYAM SUTRA

This paper is based on "Urdhva- Tiryagbhyam" sutra of Vedic multiplication, which is the most popular method for multiplication. By use of this sutra, we can make digital multiplier for binary multiplication. It is also named as "Vertically and Crosswise" method of multiplication. An illustration of this multiplication algorithm is shown in the figure below. Considering a digital hardware, a Vedic multiplier will be more power efficient and faster also as less number of steps is required for multiplication. Also there are hardly any limitations attached to this multiplication algorithm.

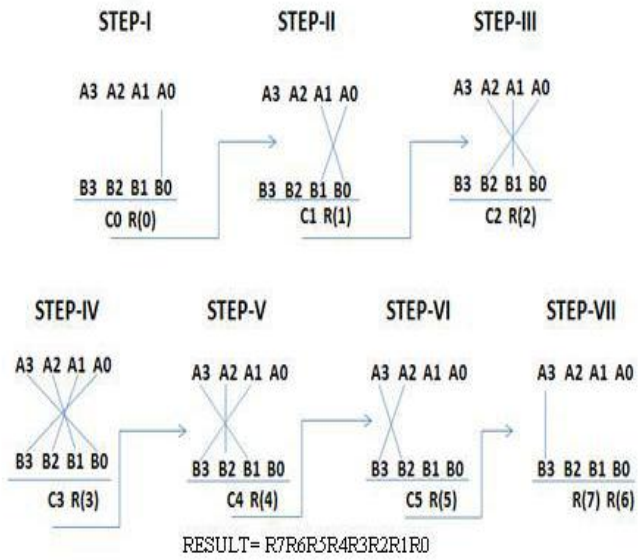


Fig: Algorithm of "Urdhva-tiryakbhyam" sutra

Consider two 4-bit binary numbers a3a2a1a0 and b3b2b1b0. Partial product (P7P6P5P4P3P2P1P0) generated are
Given by the following equations:

i. P0 = a0b0
ii. P1= a0b1 + a1b0
iii. P2 = a0b2 + a1b1 + a2b0+ P1
iv. P3= a0b3 + a1b2 + a2b1 + a3b0+ P2

v. P4 = a1b3 + a2b2 + a3b1 + P3
vi. P5 = a1b2 + a2b1 + P4
vii. P6 = a3b3 + P5
viii. P7 = carry of P6

PROPOSED DESIGN OF 2 BIT VEDIC MULTIPLIER

The 2×2 Vedic multiplier in binary is implemented by using VHDL code. In order to reduce the delay of 2×2 multiplier, it is designed by using nine full adders and a 4-bit special adder

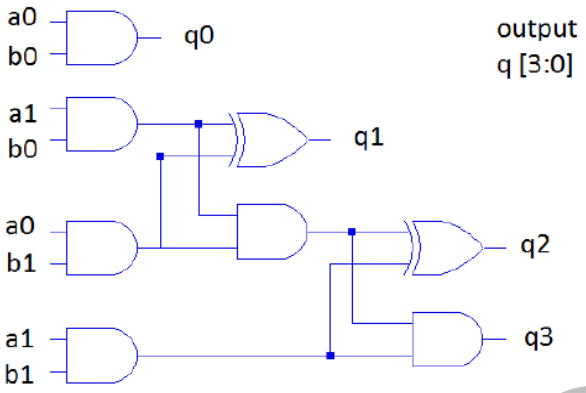


Fig1:2×2 Vedic multiplier

PROPOSED DESIGN OF 4 BIT VEDIC MULTIPLIER

The 4-bit multiplier is designed using four 2x2 Vedic multipliers which employ Urdhva Tiryagbhyam sutra and carry skip technique for partial product addition. The output of these Vedic multipliers is added by adder. In this multiplier one 4bit adder and two 6 bit adder is used. Block diagram of the proposed 4x4 multiplier is illustrated in fig.

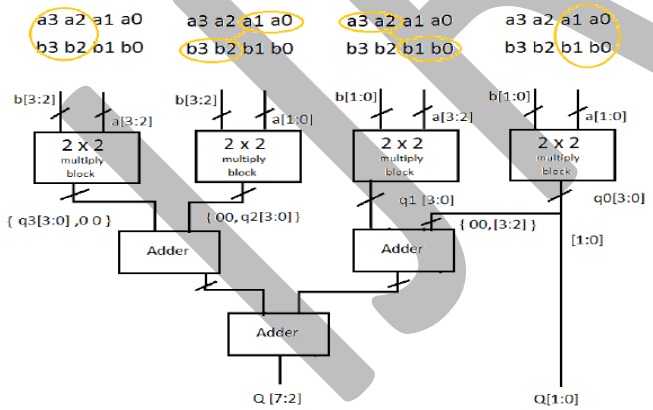


FIG2:4×4 VEDIC MULTIPLIER

PROPOSED DESIGN OF 8 BIT VEDIC MULTIPLIER

The 8-bit multiplier is designed using four 4x4 Vedic multipliers which employ Urdhva Tiryagbhyam sutra. The output of these 4-bit Vedic multipliers is added by adder. In this multiplier one 8bit adder and two 12 bit adder is used. Block diagram of the proposed 8x8 multiplier is illustrated in fig.

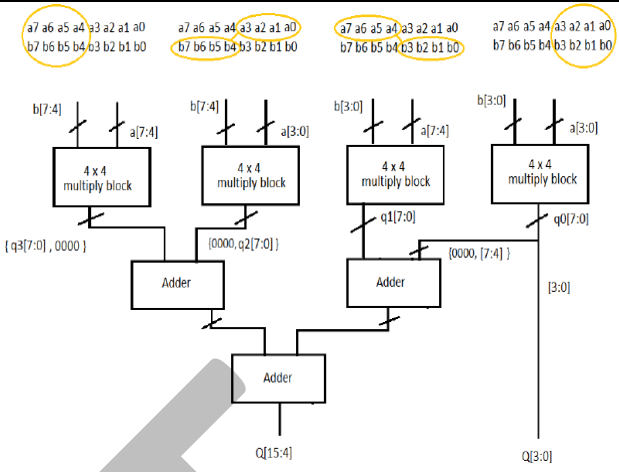
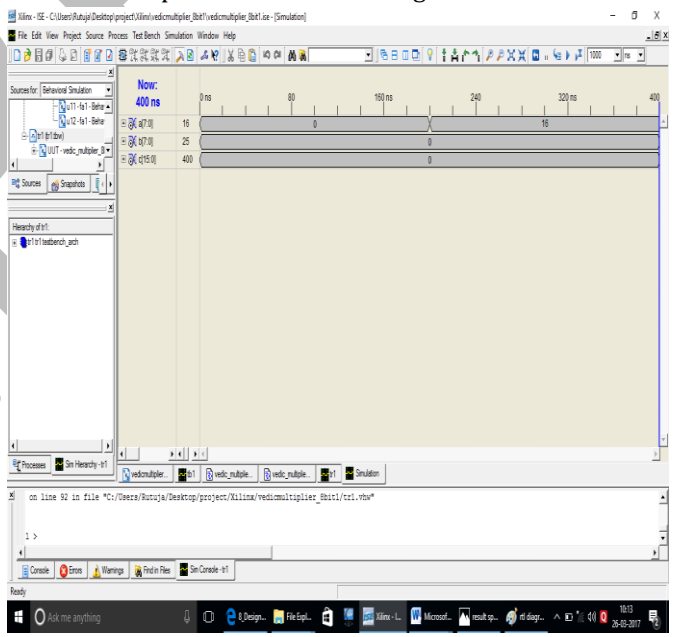


Fig3:8×8Vedic multiplier

RESULT AND DISCUSSION

The proposed 8-bit multiplier is coded in VHDL, simulated using Xilinx ISE simulator, synthesized is done in Xilinx XST for spartan3:xc3s200-5pq208 FPGA and verified for possible inputs given below .Inputs are generated using VHDL test bench .The simulator result and RTL schematic for 8-bit multiplier is shown in the figure below.



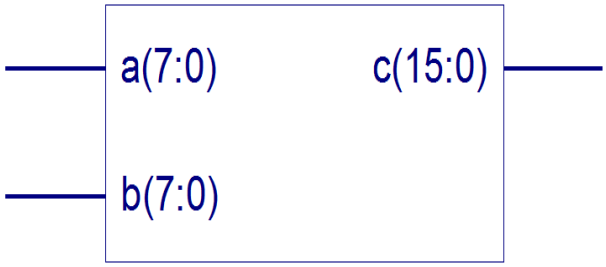


Fig4: RTL schematic

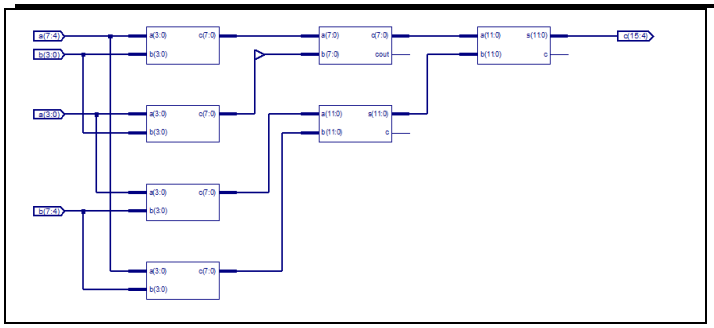


Fig5: RTL schematic

Logic utilization	used	Available	Utilization
No of slices	95	1920	4%
No of 4 input LUTs	166	3840	4%
Number of bonded IOBs	32	141	22%

CONCLUSION

This paper represents effective Vedic multiplier design using VLSI technology. Almost can be achieved using this Vedic multiplier as compared to its earlier gate level analysis or the conventional ways of multiplication. The processor's time consumption is reduced. In this paper we have achieved combinational path delay is 30.011ns. For the 8-bit Vedic multiplier and the computational complexity is also less as it is requiring few numbers of steps as compared to conventional multiplication methods.

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