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32 BIT×32 BIT MULTIPRECISION RAZOR-BASED DYNAMIC VOLTAGE SCALING MULTIPLIER WITH OPERANDS SCHEDULER

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ABSTRACT:

In this paper, a 32×32-bit multi-precision multiplier is described. The multiprecision (MP) multiplier that incorporates the variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and MP operands scheduling are used to provide a variety of operating conditions. The proposed multi-precision multiplier enables voltage and frequency scaling for low power operation. The highly dynamic voltage and frequency scaling circuits can autonomously configure the multiplier to operate with the lowest possible voltage and frequency to achieve the lowest power consumption In Previous paper PLL is used for the frequency division method. If using PLL for frequency division its hardware complexity increases. To decrease the hardware complexity and also speed is an increase is done by software using some frequency division methods. The multiplier can either work as independent smaller-precision multipliers or work as parallel to perform higher-precision multiplications. To operate at the proper precision and frequency the user's require to configure a dynamic voltage/frequency scaling management unit.

KEYWORDS: Computer arithmetic, FPGA, Scanning, dynamic voltage and frequency scaling, low power design, multi-precision multiplier.

I. INTRODUCTION:

The day by day technology increases we need compact devices which consume low power and low area. Now a days, the demand for low power, high performance portable devices has been greatly increased. In Digital Signal Processing most of the frequently used arithmetic operation is multiplication. So today's in digital signal processing a Multipliers plays an important role and also in various others application. With advanced technology, the following design targets – high speed, low power consumption and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power VLSI implementation.

Multipliers are used for applications have large area and consume considerable power. A multiplier play an important part in digital signal processing systems, like Correlation, frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), Digital Image processing etc.

While focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption. This is due to the increased demand for portable multimedia applications, which require low power consumption with high speed. Some multipliers are available like serial, parallel and serial-parallel multipliers and it is based on the way data is processed. Digital multiplier is implemented in reconfigurable device as FPGA. As we know FPGA have number of LUT's, Transistors, Registers, IO's, for effectively use of these resources, dynamic system development is necessary. Data patterns 8-bit, 16-bit, 32-bit, are mostly used in applications like graphics, audio application respectively. Hence to reduce the power it is good choice to design basic building blocks i.e. 8×8 multiplier which is faster and using less no of hardware.

II. METHODOLOGY:

The objective of this project is to implement an Dynamic voltage and frequency scaling (DVFS) for multi precision multiplier on reconfigurable FPGA (spartan6).

- To Implement of DVFS for multiplier block is on FPGA and which is offering good performance at low power supply voltage 1.25V to 3.3V and at frequency 25MHz to 100MHz.
- To avoid the unnecessary switching activity dynamic voltage and frequency scaling is done.
- To generate control signal, input data scanning is carried out.

The following figure shows the operation of the multiplier system.

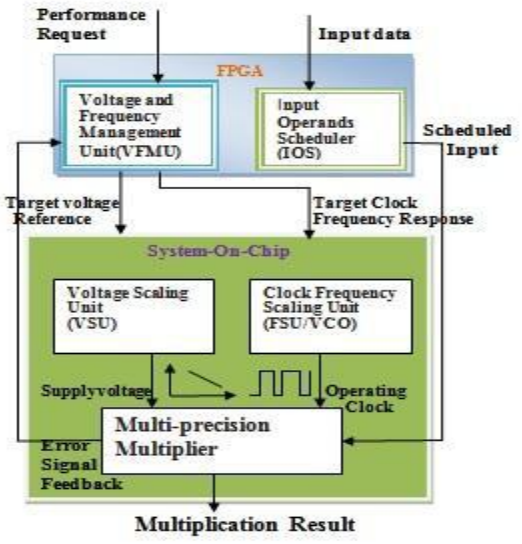

Fig 1.Overall multiplier system architecture

The proposed Multiprecision multiplier system contains five different modules are as follows:

1) The Multiprecision multiplier.
2) Input scanning is to detect the range of input operands scheduler, according to the scanned data it sends the control signal to voltage and frequency management unit.
3) Voltage scaling takes place according to current input bit streams scanned by scanning module, and scale voltage to reduce the power consumption.
4) Frequency dividers are the building block of digital circuit by using JK f/f frequency scaling for 8,16,32-it as, quadrant of main frequency, half of main frequency and main frequency.
5) Multiplication operation is done at various levels as the control signal.

1) SCANNING:

Scanning is for making system dynamic. This is the first and important step, by this step input range is detected. The scanning of input data from LSB to MSB. to detect the range. The scanning is byte wise i.e., 0 to 7, 8 to 15, 16 to 32. After the scanning it will generate the control signal 1, 2, 3 for 8bit, 16bit, and 32bit data. If there is combination of 8×16, 8×32, 16×32, then highest priority will be selected and control signal is generated. As we know the maximum range of 8- bit, 16-bit, 32-bit, is 2^7=128, 2^15=32768, 2^31=2147483648. These are the threshold values for system according to this control signal generated. This control signal sends to the frequency and voltage management unit. Xilinx 14.5 ISE is used for simulation.

Algorithm for scanning of input data to the system.

Step 1. Start

Step 2.Input given to the system.

Step 3.Depending upon the values of input oprands for m1 and m2 are entered and the control signals are generated.

- If oprands are lower than or equal to 128 i.e.data is of 8bit then control signal will be 1.
- If oprands are lower than or equal to 32768 i.e data is of 16bit then control signal will be 2.
- If oprands lower than or equal to 2147483648 i.e data is of 32bit then control signal will be 3.

Step 4.If input is a combination of different data then highest

priority will be selected and control signal will be generated.

Step 5.This genetrated control signal given to VFMU.

Simulation result of 8-bit, 16-bit,32-bit data are as shown in below.

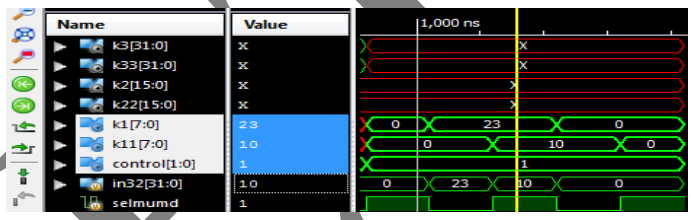

Fig.2. Scanning result for 8bit data.

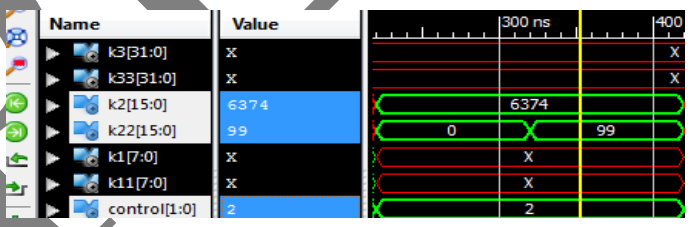

Fig.3. Scanning result for 16 bit data.

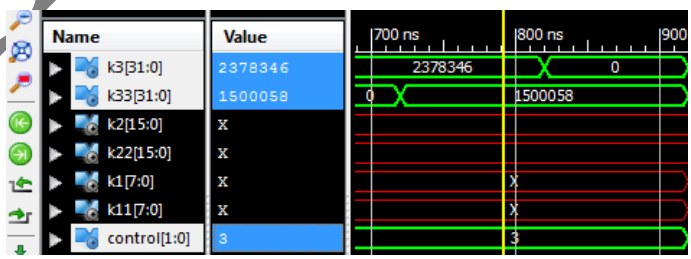

Fig.4. Scanning result for 32 bit data.

As in fig.2 shows that both input operands are 23 and 10 i.e. below 128 so control signal is 1 in this case. In fig.3. Input operands are 6374 and 99 which are below 32768 so it is 16-bit data and control signal is 2. In fig.4.oprands are 2678346 and 1500058 are 32-bit data and lower than 2147483648 so, control signal is 3.

2) FREQUENCY SCALING:

Dynamic frequency scaling is a technique in system architecture where by frequency of the system can be automatically adjusted "on the fly", either to conserve power or to reduce the amount of heat generated by the

chip. In that, frequency scaling is used to conserve the power.

Algorithm for frequency scaling according to control signal.

Step 1. Start.

Step 2.Control signal generated from Input scanning, as input data is given to the system.

Step 3.VFMU sends targeted reference frequency to frequency scaling unit.

Step 4.Control signal can be 1, 2, and 3 decision will take place according is as follows.

- If control signal is 1 then scanned data is of 8-bit frequency scaled down to f_8=F/4 i.e. 25MHz
- If control signal is 2 then scanned data is of 16-bit frequency scaled down to f_{16}=F/2 i.e. 50MHz
- If control signal is 3 then scanned data is of 32-bit frequency is f_{32}=F i.e. 100MHz.

Step 5.Scaled frequency sends to Multiprecision multiplier for operation.

Simulation result of JK Flip-Flop as shown in below figure.

We can done the frequency scaling using JK FF. It's the simple process. Frequency is divided by 2 require only one JK FF and frequency divided 4 require the Two JK FF. In our project require frequency division by 2 and 4.

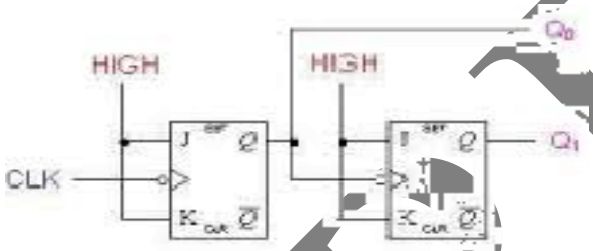

Fig 5. Block diagram of frequency division by JK FF.

The frequency scaling using JKFF is better than the other methods. Frequency scaling using JK FF require only 2 registers and 3 Slice LUT and delay is 4.202 ns.

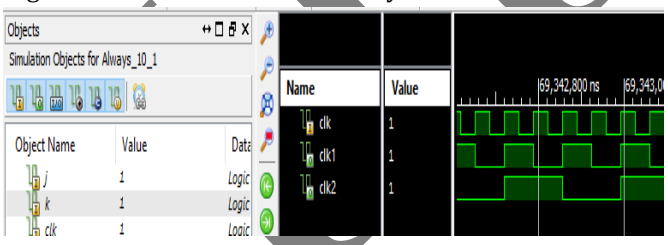

Fig.6. Simulation result of frequency scaling by JK flip flop

But T FF require less delay as compare to JK but require 4 registers and 4 Slice LUT. Then the JK FF frequency method is used in 32x32 multiplier.

3) VOLTAGE SCALING:

At the time of implementation of integrated circuits(IC) the manufacturer kept the fixed word length that is not used in all the application. In case if IC is of 32bit current operation is of 8bit then IC uses full word length and voltage, due to this unnecessary voltage used for per operation. To avoid this voltage scaling is important according to workload to system. In power optimization technique a Dynamic voltage scaling is important. For low power technique Dynamic voltage and frequency scaling is very popular. In this system voltage scaling is done by Multiprecision multiplier. In the system scanning is done to detect and generated control signal, that signal indicates the current workload according to that system changes its voltage dynamically. Voltage scaling is done according to the control signal given to voltage scaling unit.

Algorithm for voltage scaling according to the control signal.

Step 1.Start.

Step 2.VFMU sends targeted reference voltage to voltage scaling unit.

Step 3.VFMU sends targeted reference frequency to frequency scaling unit.

- If control signal is 1 then scanned data is of 8-bit voltage automatically switched to 1.2V.
- If control signal is 2 then scanned data is of 16-bit voltage automatically switched to 2.5V.
- If control signal is 3 then scanned data is of 32-bit voltage is 3.3V.

Step 4. Voltage signal sends to Multiprecision multiplier for operation.

Step 5. Using that voltage, multiplication is carried out and finally result of operation is display on LCD.

4) MULTIPLICATION:

In this system voltage and frequency scaling is done for MP Multiplier as an application .Multiplication operation is performed on different input data bit ,32bit,16bit,8bit. Multiplication is on different combination of data then voltage and frequncy adaption according to highest priority of data.The Multiplier is controlled by three external signals.Once the input is scanned and detected the operating voltage and frequncy are tuned automatically.The voltage range and frequency of 1.2-3.3V and 32-8MHz is achived for full functionality respectively. Operation can be perfomed on different data bit, 8×8, 8×16, 16×16, 8×32, 16×8, 16×32, 32×32, 32×16. The Delay in lower bit operation is lower as compare to other higher bit opration condition.

EXPERIMENTAL RESULT:

SYSTEM IMPLEMENTATION:

The FPGA Spartan 6E is used for implementation of dynamic system in terms of voltage and frequency. Input is given to system it can be given by user it processes that detect the according to that frequency and voltage range scaled and results displays on LCD. 4-Bit counter is

implemented for effectively analyzing frequency scaling on the hardware kit. As scaled frequency for 8-bit is 25MHz, counter blinking rate is slower than at 50MHz or 100MHz. LED blinking is totally depends on the magnitude of frequency. Voltage scaled output is display by LCD.

LCD showing multiplication results for different input data bit a and b are multiplicand and multiplier with corresponding voltages and frequencies.

From the literature survey it can be stated that, spurious signal generation is results of long chain of traditional adders used in multiplication.

III. CONCLUSION:

This paper presented a novel technique for efficient use of hardware resources (area) to reduce power on FPGA. By scaling technique here dynamically adjusting the frequency and voltage according to the bit width of the input data. As input is known the system can save the power by disabling the unused section of multiplier. Dynamic systems uses only required number of gates as input is scanned for real application by adjusting voltage and frequency, so area and power will be saved. This saving is largely due to the reductions in the reconfigurable interconnection required, which normally dominates the die area of typical FPGA.

IV. FUTURE WORK:

The work can be expanded for implementation of integrated circuit IC which works on various data input ranges i.e. 4 bit, 8-bit, 16-bit, 32-bit, 64-bit, 128-bit and so on. Such systems with dynamically adjusting voltage and frequency for operation will be the help to increase performance in terms of power and area (hardware resources).The use of such system is suitable in various embedded multimedia and DSP applications with flexible processing ability and low power consumption will takes place it will be great power optimization technique.

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