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FPGA BASED SDR FOR DPLL APPLICATION

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ABSTRACT:

To design and develop a system on chip reconfigurable modules Field Programmable Gate Array (FPGA) provides a way with high performance. In this paper, FPGA architecture is proposed, which would be a starting point for developing an efficient Software Defined Radio (SDR) architecture for recovering audio signals from digitally modulated frequency wave. At the modulator and demodulator sections, a Digital Frequency Generator (DFG) is applied for generating the carrier wave by exploiting the quarter wave symmetry of sine or cosine waves with dynamic range of more than 90dB.

KEYWORDS: DFM, DPLL, FPGA, SDR.

I. INTRODUCTION:

The advances in the technologies of wireless communication, needs of customer also increased to communicate from any place with different accessories. This advancement in the wireless communication leads to evolution of very efficient radio receivers. Software defined Radio (SDR) affords an attractive nature of reconfigurable and Multimode operation. SDR is nothing but a collection of Hardware and software, in which all the radio functions can be implemented using software coding or firmware on a processing system. Software Defined Radios are transceivers that turn PCs and chassis into next-generation wireless prototyping tools. Use these products for designing wireless communication systems, physical layer prototyping, and performing signals intelligence research. According to the applications in the communication system this software can be alterable. The processing systems suggested above can be any of the following, Field Programmable Gate Arrays (FPGA), Digital Signal Processors (DSP), General Purpose Processors (GPP), Programmable System on Chip (SoC) or other Application Specific Programmable Processors. Software Defined Radio (SDR) is a recently evolved technology i.e. implemented by signal- processing software running on generic hardware platforms. It makes the system more flexible, adaptive and that's why it can be used to solve many of the problems faced by traditional hardware-based radio systems. In general, Field Programmable Gate Array (FPGA) is employed as the hardware platform for many of the real time signal processing systems due to its high performance, less power consumption and configurability. The plan is to move the analog Frequency Modulation (FM) to digital which leads to the development of Digital Audio Broadcasting (DAB). DAB uses a coding technique and the most effective Orthogonal Frequency Division Multiplexing (OFDM) techniques which is fully in the digital envelope. This system demands the entire analog FM system have to be switched off. The DAB using OFDM was first implemented in United Kingdom (UK) but it turned out to be a failure [5]. So, the new approach is to efficiently convert the FM to digital form which is meant by Digital FM (DFM) using fast switching ADC. Non linearity of the analog Voltage Controlled Oscillator (VCO) affects the clarity of the signals over certain frequency range and hence it is to be replaced with Digital Phase Locked Loop (DPLL). DPLL is nothing but electronic feedback system which is used for signal generation. DFM techniques are used to get optimum performance and accurate audio fidelity in any audio broadcasting system which also includes Direct To Home (DTH) services.

II. LITERATURE REVIEW:

In [1], Neenu Joseph, Dr. P Nirmal Kumar describes the design and implementation of OFDM transmitter and Receiver in Partial Reconfigurable (PR) FPGA for Software Defined Radio (SDR) system. Blocks of PR inside FPGA helps in reducing the complexity in SDR system design, overall power and area consumption.

Jobin Varghese, Luxy Mathews [2], describes a FPGA architecture for recovering audio signals from digitally modulated frequency wave is proposed, which would be a starting point for developing an efficient Software Defined Radio (SDR) architecture.

Amiya Panda, Debahuti Mishra, and Hare Krishna Ratha, [4] proposes a field-programmable gate array (FPGA)-based software defined radio (SDR) implemented (FTS). The applied design procedure replaces a multiple platform-based system with a single platform. FTS basically involves in generation and transmission of remote command signals to the airborne FV to execute some operation inside the vehicle as required.

Chris Dobson, Kurt Rooks [3], In this ARM core and FPGA hybrid platform is used. The ARM core provides

all of the benefits and ease of use common to modern high-level software languages while the FPGA segment offers high performance for computationally intensive components of the application.

III. METHODOLOGY:

The demodulation architecture of DPLL consists of the basic building blocks as shown in Figure 2. The DFM modulator consists of four basic sections. These sections are namely Phase Detector, Loop Filter, Digital Frequency Generator and Finite Impulse Response Filter. With no input signal, control voltage for the Digital Frequency Generator (DFG) is equal to zero that operates at a set frequency, which is the free running frequency. By applying an input signal to the system, the phase detector compares the phase and frequency of the input signal with the DFG frequency and produces an error voltage. This gives the relationship between phase and the frequency of two signals.

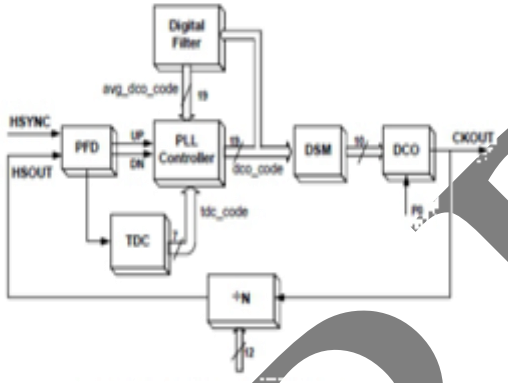


Fig (1). Block Diagram of DPLL

The Phase Locked Loop (PLL) is used as a frequency synthesizers or clock generators. A PLL is nothing but a feedback system comparing input phase with output phase that produces a signal that is in phase with the input signal. But when it is used as pixel clock generator in digital video display systems as analog interface, it needs to phase align the output with a noisy and very low frequency of horizontal synchronization signal. If proper phase aligning is not obtained, the displayed image will become blurry. For such applications the PL must closely track the input clock signal.

Figure 1 demonstrates the block diagram of the DPLL, which is composed of a Phase Frequency Detector, Time to- Digital Converter (TDC), a first-order delta-sigma modulator(DSM), digitally controlled oscillator (DCO), PL controller, a digital loop filters (DLF) and a 12 bit programmable frequency divider (Pre-scalar). The HSYNC (Horizontal synchronization clock) is taken as the reference clock, and the HSOUT is the output pixel clock (CKOUT) divided by the frequency divider. The frequency multiplication ratios for different video display resolutions are specified by display monitor timing standard. Based on different display standards 12 bit frequency divider is programmed externally.

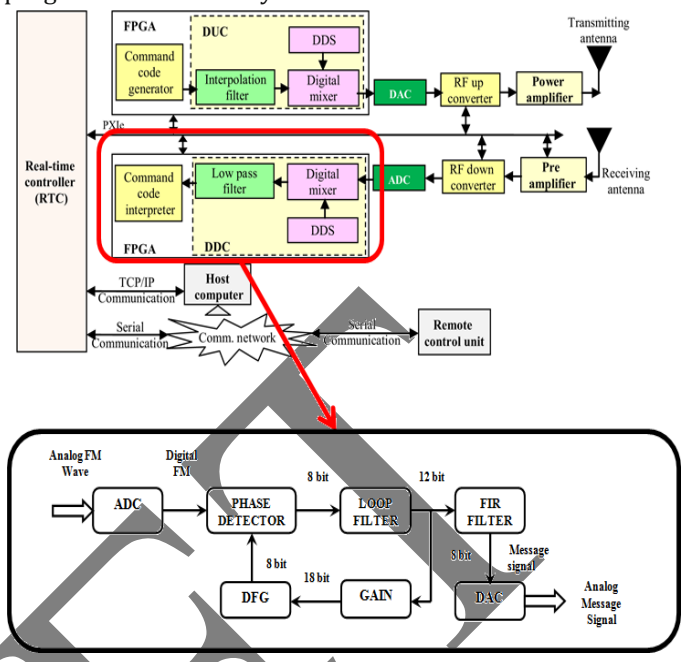


Fig (2). DPLL Architecture

A. PHASE DETECTOR:

Phase Detector (PD) determines phase error between input signal and output signal generated by DFG. This operation employs a multiplier module. The input signal is frequency modulated, so the input signal, M(n) can be expressed as follows.

$$M(n) = \sin(wn + \theta) \quad (1)$$

Feedback loop mechanism of the DPLL will force DFG to generate cosine signal, U(n) with same frequency of the input signal

$$U(n) = \cos(wn + \varphi) \quad (2)$$

Output of phase detector is product of these two signals, using familiar trigonometric identity gives.

$$E_d(n) = K_m * [\sin(wn + \theta)\cos(wn + \varphi)] \quad (3)$$

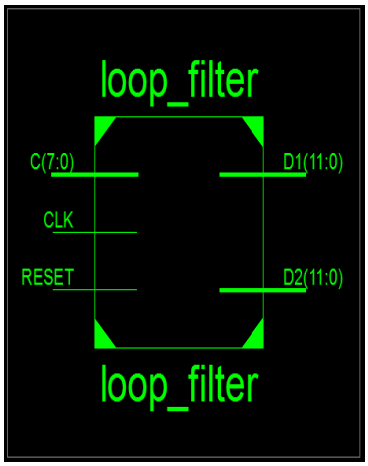
$$E_d(n) = .5 * K_m * \sin(2wn + \theta + \varphi) * \sin(\theta - \varphi) \quad (4)$$

B. LOOP FILTER:

Loop filter has important in the operation of phase locked loop. The choice of the circuit values here is carefully compromise between a number of conflicting requirements.

The PLL filter is used for removal of any unwanted high frequency components which pass out of the phase detector that appear in the VCO tune line. To show this a mixer is used as a phase detector. When the loop is in lock state the mixer will produce two signals. These signals are sum and difference frequencies. As these two signals entering the phase detector have the same frequency. The sum frequency will fall at a point equal to twice the frequency of the reference. The difference frequency is zero and a DC voltage is proportional to the phase difference as expected. If this signal is not attenuated it will

reach the control voltage input to the VCO which give rise to spurious signals. The loop filter has the ability to affects the loops that change frequencies quickly. If the filter has a very low cut-off frequency then this changes in tune voltage will take place slowly, and the VCO will not be able to change its frequency as fast.



Fig(3). RTL View of structure of loop filter

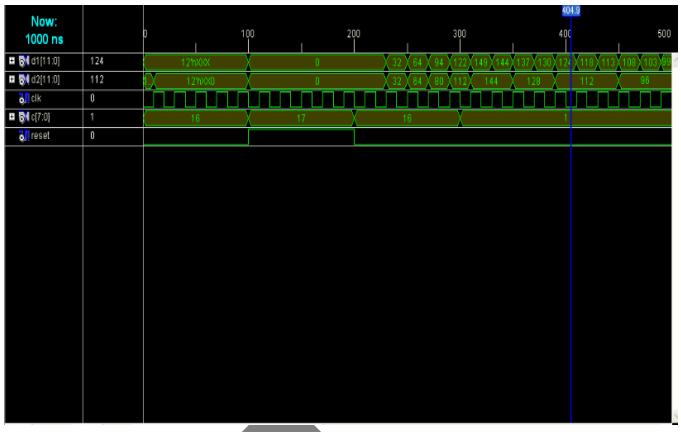
B. DIGITAL FREQUENCY GENERATOR:

The digital frequency generator (DFG) consists of a shift register, an adder, a latch and a 1M bit EPROM. The shift register reduces the need of port pins of the MCU and also synchronizes the data input from the MCU with adder's operation. The output of adder is feedback to itself via the latch. Therefore the value of the latch output is increased by the value in the shift register at every clock cycle. This value is taken as an address to the EPROM and this EPROM contains a table, which allows to conversion of the value from the latch into the amplitude of the output signal. In short any waveform can be stored and generated. The accuracy of the generated frequency is determined at low frequencies by oscillator's precision. At high frequencies by the jitter, this is caused by the discrete nature of adder and table. The frequency and amplitude modulation is based on DDS software on microcontroller. Since the sinus is read from a 16 KB lookup table (LSB first) starting at &H01000, which can replace by any other waveform.

B. FINITE IMPULSE RESPONSE FILTER:

A finite impulse response filter (FIR) is said to a filter which has a finite duration impulse response and it settles to zero in finite time. This FIR filter is in contrast with infinite impulse response filters (IIR), which have internal feedback and may continue to respond indefinitely. Before settling to zero, the impulse response of an Nth-order discrete-time FIR filter lasts for N + 1 sample.

IV. RESULT:



Fig(4). Simulation Result

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	19	3584	0%
Number of Slice Flip Flops	24	7168	0%
Number of 4 input LUTs	23	7168	0%
Number of bonded IOBs	34	221	15%
Number of GCLKs	1	8	12%

V. CONCLUSION:

The designed architecture provides an optimization in phase detector component to achieve smaller circuit area. Digital Phase locked loop is an interesting topic for the research, as it has covered various disciplines such in communication theory, control theory, signal analysis, design with transistors and op-amps, digital circuit design and non- linear analysis.

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