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ABOUT TESTING DIGITAL DEVICES BY REFERENCE TESTS

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ABSTRACT:

The article discusses one of the innovative ways of testing digital devices, the method of reference tests. A mathematical model of the testing process according to the proposed method is described.

Keywords: diagnostics of digital devices, localization of faults, sequence of control tests, reference test, reference state, simulation.

INTRODUCTION:

The method of diagnosing the specialized state of equipment components and congregations, in specific, test diagnostics, is one of the foremost complex and time-consuming operations that go with the item at all stages of the life cycle of computerized components of data communication (ICS) and data control (ICS) frameworks. Advancement of the mechanical base made it conceivable to utilize the VLSI premise (programmable rationale coordinates circuits - FPGAs (PLD, FPGA), frameworks on a chip (SoC), advanced flag processors - DSPs (DSP)) when making advanced computerized gadgets and frameworks, containing the number valves of the arrange of 105 .. .107. This drastically complicated the arrangement of issues of specialized diagnostics due to the increment within the measurement, usefulness and sort of surrenders of the objects of diagnostics (OD). Therefore, the rummage around for a arrangement to numerous particular problems of specialized diagnostics of computerized components of ICS and IMS, taking into consideration the specifics of the advanced innovative premise, measurement, speed and other variables, is still an pressing errand [1]. The pith of test diagnostics comprises in applying test impacts to the inputs of the advanced gadget beneath test (DC), perusing real answers from its yields and comparing the last mentioned with the reference ones. As a rule, the reference response is the output sequence of signals obtained for the same type of serviceable control center or its simulation model [2].

Let us denote by v and z the number of primary inputs and outputs of the tested control center, respectively, and by n - the total number of control tests. Diagnostics of the control center using the simulation method is as follows. A set of input control tests $X = \{x_{ij}\}$, $i = \overline{1, v}$, $j = \overline{1, n}$,
$x_{ij} \in \{0,1\}$, such that any malfunction in the circuit will manifest itself in the reaction $R = (r_1, r_2, ..., r_z)$, $r_i \in \{0,1\}$, removed from its output and is detected as an erroneous sequence $G = (g_1, g_2, …, g_z)$. The erroneous sequence is defined as $G = R \oplus R_e$, where R_e is the reference response obtained by simulation of the same type of operational control unit.

MAIN PART:

In the case when the equality $G = (0,0, ..., 0)$ is fulfilled for all $j \in [1, n]$, the investigated control center is considered to be operational. Otherwise, it is declared faulty and the procedure for localizing the detected faults is performed.

Let us assume that as a result of carrying out k control tests, a discrepancy is established between the output signals of the model (the reaction of the reference control center) and the tested control center, i.e. $G \neq (0,0, ..., 0)$. Traditionally, the fault localization procedure

consists in multiple re-feeding to the inputs of the tested control unit of a sequence of k control tests and comparing all output signals of all elements of the control unit, as well as the input signals of the control unit with the corresponding signals in a working model. A faulty element is one that detects, with correct input signals, a discrepancy between the output signal and the reference signal received on the model from at least one output. However, such an organization of the process of localizing the detected faults is very laborious even for a control center with a low level of complexity.

In this regard, we propose to start the diagnostic troubleshooting with some intermediate i-th (i <k) control test, having previously established the internal state of the model corresponding to the state of the control center after the i-1 th control test.

To achieve this goal in the modeling process, it is necessary to provide for the formation and storing in the memory of the control PC of an automated control and diagnostic system (ASKiD) of intermediate reference tests of the diagnosed control center [3,4].

The reference test (OT) is a control test for which the internal state of the control center model is memorized, which is formed after passing all previous control tests, starting with the first one.

The reference state of the control center model means its internal state corresponding to the OT. Reference states (OS) are formed by carrying out a single set of control tests on a serviceable model of the diagnosed control center. The number of operating systems formed is selected depending on the complexity level of the diagnosed control center, the size of control tests, as well as the number of faults in the circuit. Too many of them are associated with the time spent on memorizing the corresponding internal states of the model, too few - the time spent on conducting a number of tests, from the reference one to the test that detects a malfunction. At the same time, the ratio i <k takes place and i is selected taking into account the fact that when diagnosing faults in digital sequential circuits, it is not enough to simulate the test with which the fault was detected, since in this case, the simulation results of each test are characterized by the results of the previous tests. If there is an ASKiD in the memory of the control PCs, intermediate OTs of the diagnosed control center for the formation of standards, the nearest OS is installed on the model and the simulation is performed only within the testing interval from the reference one to the test that detected this malfunction.

Mathematical model of the testing process:
Let us introduce the following notation:

Tav- the average value of the total testing time on the simulation model of the control center, taking into account the formation of OT;

N is the average number of contacts (the number of the probe position) for the control center elements checked during the fault localization;

n is the total number of control tests;

m is the total number of selected OTs;

t_0 is the time spent on the formation of one OT (memorizing the internal state of the model in the PC memory);

t_Y - time spent on establishing the internal state of the control center model;

τ is the average time of passing the test;

γ is the total number of control center malfunctions detected by a given set of control tests;

α is the loss factor, defined as the proportion of redundant control tests carried out due to the need to start modeling from the last (before the failure is detected) FROM (0≤α≤1);

k_I - the number of control tests carried out between the (i-1) -th and i-th OT;
p (k_I) is the unconditional probability that the fault will be localized at the i-th testing interval, i.e. that it is detected by control tests located between OT i-1 and i.
According to the proposed method, testing the control center is carried out with the help of OTs formed by a single passage of n control tests on a working model of the diagnosed control center.

In this case, the total time of mt_0 formation is :

$$\sum_{i=1}^{m} t_0 = mt_0, \qquad (1)$$

and the total time for passing n control tests is:

$$\tau \sum_{i=1}^{m} k_i = \tau n. \qquad (2)$$

The time of diagnostic troubleshooting, detected on the i-th testing interval, is expressed as:

$$Nt_y \sum_{i=1}^{m} p(k_i) + N\alpha\tau \sum_{i=1}^{m} k_i p(k_i) = Nt_y + N\alpha\tau \sum_{i=1}^{m} k_i p(k_i), \qquad (3)$$

where the first term expresses the average time to establish the internal (reference) state of the model, corresponding to the last (before the detection of a malfunction) OT, in the process of checking the inputs (outputs) of the control center elements. The second term in expression (3) expresses the time spent on repeating control tests, starting from OT, during the diagnostic troubleshooting.

Thus, taking into account expressions (1), (2) and (3), the average value of the diagnostic testing time t_{av} spent on the simulation model, according to the proposed OT method, is expressed as

$$T_{cp} = mt_0 + n\tau + \gamma N(t_y + \alpha\tau \sum_{i=1}^{m} k_i p(k_i)).$$

This allows you to significantly reduce the time of fault localization and the required amount of RAM on the ASKiD PC.

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